WHAT IS CLAIMED IS:

1. A method of forming a semiconductor device, comprising:

simultaneously forming first electrodes adjacent each other on a substrate;

forming a dielectric layer between the first electrodes; and

creating a second electrode between the first electrodes, the second electrode contacting the dielectric layer between the first electrodes to thereby form adjacent interdigitated electrodes.

2. The method as recited in Claim 1 further including producing a first conductive layer over the substrate prior to simultaneously forming and wherein simultaneously forming includes simultaneously forming the first electrodes on the first conductive layer, the conductive layer interconnecting the first electrodes.

3. The method as recited in Claim 2 wherein forming a dielectric layer includes forming the dielectric layer over and between the first electrodes and creating a second electrode includes creating an electrode layer over and between the first electrodes to form interconnected second electrodes over and between the first electrodes.

4. The method as recited in Claim 1 wherein simultaneously forming includes patterning a sacrificial layer on the substrate, forming the first electrodes adjacent each other within the patterned sacrificial layer and on the substrate, and removing the sacrificial layer.

5. The method as recited in Claim 1 further including producing a first conductive layer over the substrate prior to simultaneously forming and wherein simultaneously forming includes patterning a sacrificial layer on the substrate, forming the first electrodes adjacent each other within the patterned sacrificial layer and on the substrate, and removing the sacrificial layer.

6. The method as recited in Claim 1 further including forming a first barrier layer between the first electrodes prior to forming the dielectric layer between the first electrodes and forming a second barrier layer between the first electrodes prior to creating a second electrode between the first electrodes, the second electrode contacting the barrier layer between the first electrodes.

7. The method as recited in Claim 1 wherein simultaneously forming includes simultaneously forming first electrodes having an

aspect ratio ranging from about 7:1 to 10:1 adjacent each other on a substrate.

8. A method of manufacturing an integrated circuit, comprising:

forming active or passive devices over a substrate;

creating an interdigitated capacitor over the substrate, including:

placing a first conductive layer over the substrate,

simultaneously forming first electrodes adjacent each other on the first conductive layer, the conductive layer interconnecting the first electrodes,

forming a dielectric layer over and between the first electrodes and on the first conductive layer, and

depositing an electrode layer over and between the first electrodes to form interconnected second electrodes over and between the first electrodes; and

interconnecting the active or passive devices and the interdigitated capacitor to form an operative integrated circuit.

9. The method as recited in Claim 8 wherein simultaneously forming includes patterning a sacrificial layer on the substrate, forming the first electrodes adjacent each other within the patterned sacrificial layer and on the substrate, and removing the sacrificial layer.

10. The method as recited in Claim 8 further including forming a first barrier layer between the first electrodes prior to forming the dielectric layer over and between the first electrodes and on the first conductive layer and forming a second barrier layer between the first electrodes prior to depositing an electrode layer over and between the first electrodes to form interconnected second electrodes over and between the first electrodes, the electrode layer contacting the second barrier layer.

11. The method as recited in Claim 8 wherein simultaneously forming includes simultaneously forming first electrodes having an aspect ratio ranging from about 7:1 to 10:1 adjacent each other on a substrate.

12. The method as recited in Claim 8 wherein forming a dielectric layer includes forming a dielectric layer having a high dielectric constant.

13. The method as recited in Claim 8 wherein creating an interdigitated capacitor includes creating an interdigitated capacitor wherein the first electrodes and the first conductive layer are comprised of substantially the same material.

14. The method as recited in Claim 8 wherein creating an interdigitated capacitor includes creating an interdigitated capacitor wherein the first electrodes, the first conductive layer, and the electrode layer are comprised of substantially the same material.

15. An interdigitated capacitor, comprising:

first electrodes located on and interconnected by a first conductive layer;

a dielectric layer located over and between the first electrodes and on the first conductive layer; and

an electrode layer located on the dielectric layer and over and between the first electrodes to form interconnected second electrodes over and between the first electrodes.

16. The interdigitated capacitor as recited in Claim 15 further comprising a first barrier layer located between the first electrodes and the dielectric layer, and a second barrier layer located between the dielectric layer and the electrode layer.

17. The interdigitated capacitor as recited in Claim 15 wherein the first electrodes have an aspect ratio ranging from about 7:1 to 10:1.

18. The interdigitated capacitor as recited in Claim 15 wherein the dielectric layer is comprised of a material having a high dielectric constant.

19. The interdigitated capacitor as recited in Claim 15

wherein the first electrodes and the first conductive layer are comprised of substantially the same material.

20. The interdigitated capacitor as recited in Claim 15 wherein the first electrodes, the first conductive layer, and the electrode layer are comprised of substantially the same material.